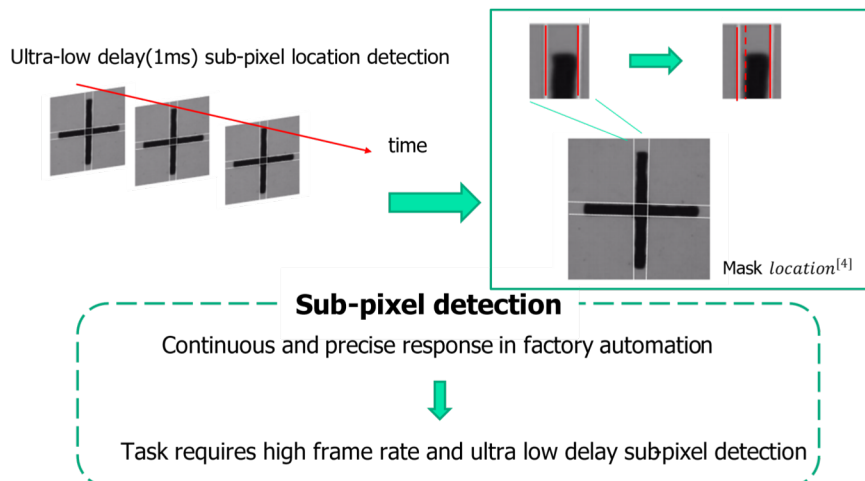


# Directional DCT-Correlation with Monotonous Estimation for High Frame-rate and Ultra-low Delay Sub-pixel Location Detection

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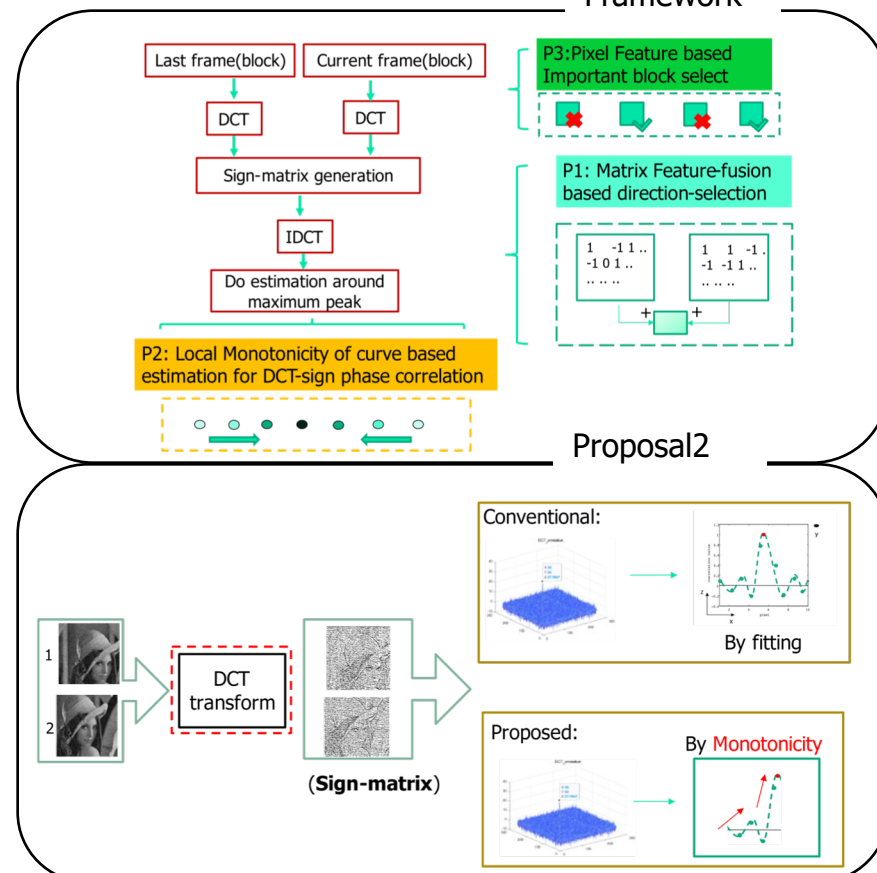
## Background

### Sub-pixel location detection



## Proposal

### Framework



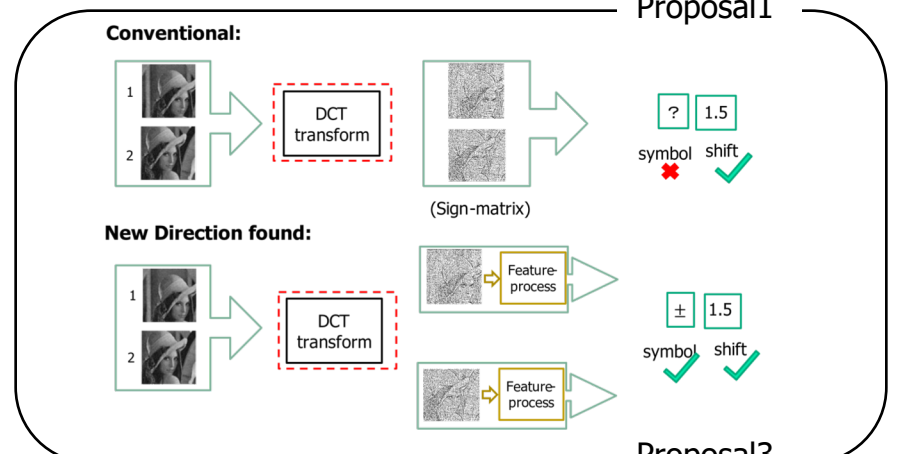
## Target

- Implement high frame rate and ultra-low delay sub-pixel location with FPGA

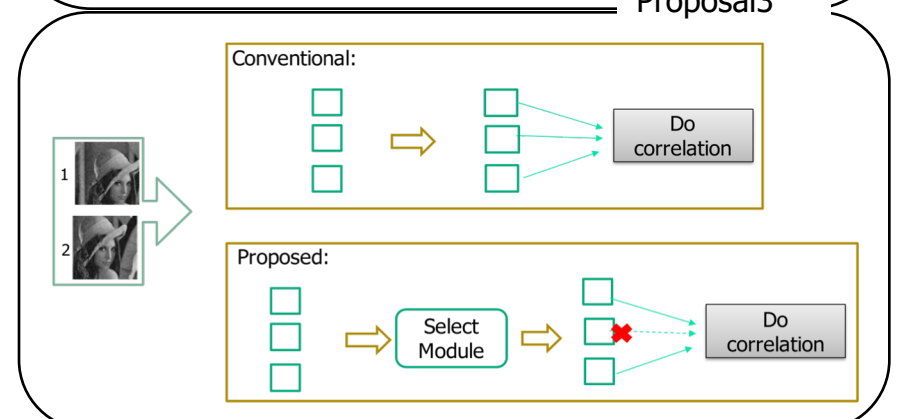
## Challenge

- Redundant calculation for block
- Loss of some information for direction
- Complex fitting function for estimation

### Proposal1



### Proposal3



## Evaluation result

### Software

Direction X

	POC(Block)		DCT-sign correlation		P1+P2+P3	
	AVG	$\partial$	AVG	$\partial$	AVG	$\partial$
64*64	-0.29	0.49	3.25	0.173	0.432	1.18
96*96	-0.27	0.54	3.19	0.183	0.38	0.92
128*128	-0.32	0.67	3.28	0.167	0.416	1.05

### Hardware performance:

- Processing time: 0.75ms/frame

Memory	
FF(Flip Flop)	50053(12.28%)
LUT	35216(17.28%)
BUFG	1(3%)
IO	194(38.8%)
DSP	48(5.71%)

## Conclusion

- 1. Algorithm with proposal1 improves the result from negative number to positive
- 2. Implemented algorithm for high frame rate an ultra-low delay sub-pixel location detection achieve the 0.75ms/frame



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